

illustration specific preferred embodiments in which the disclosure [inventions] may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice them [the invention], and it is to be understood that other embodiments may be utilized and that mechanical, chemical, electrical, and procedural changes may be made without departing from the spirit and scope of the present disclosure [invention]. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the present invention is defined only by the appended claims.

The paragraph beginning on page 5, line 9 is amended as follows:

Embodiments of the [The] present invention provide [provides] a solution to package density constraints in the form of dimension design rules that specify minimum sizes of terminals on IC substrates, as well as minimum width and spacing of traces on the substrate. Various embodiments are illustrated and described herein.

The paragraph beginning on page 6, line 5 is amended as follows:

FIG. 1 is a block diagram of an electronic system 1 incorporating at least one electronic assembly 4 with a high density interconnect, in accordance with one embodiment of the invention. The high density interconnect of embodiments of the present invention can be implemented at one or more different hierarchical levels, e.g. at the chip packaging level or at the PCB level.

The paragraph beginning on page 6, line 10 is amended as follows:

Electronic system 1 is merely one example of an electronic system in which embodiments of the present invention can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

The paragraph beginning on page 13, line 10 is amended as follows:

While the embodiments illustrated in FIGS. 4-8 have been described in terms of IC dice coupled to IC substrates, embodiments of the invention are [is] not limited to coupling an IC die to an IC substrate. They [It] can be implemented in any electronics package in which it is desired to increase the escape density of traces. For example, the precepts of the invention can be applied to coupling an IC package to a substrate such as a PCB or motherboard, or to any other type of packaging element. Embodiments of [The] invention can also be applied to coupling IC dice to land grid array (LGA), pin grid array (PGA), or chip scale package (CSP) substrates, or the like.

The paragraph beginning on page 14, line 22 is amended as follows:

A significant advantage of embodiments of the present invention is that any embodiment in which the effect of the bump pad dimension is minimized or is even eliminated enables the maximum trace escape density to be achieved. This can be accomplished with embodiments such as those illustrated in FIGS. 4-9.

The paragraph beginning on page 17, line 4 is amended as follows:

The present disclosure [invention] provides for an electronic package with high density interconnect, in several different embodiments, and for methods of manufacture thereof, that maximize trace escape density. Embodiments have been disclosed in which the trace density can reach the geometrical limit of the reciprocal of the pitch. An IC package and/or PCB that incorporates the high density interconnect features of the present disclosure [invention] has reduced physical dimensions and is capable of performing with enhanced electronic performance, and such systems are therefore more commercially attractive. Further, embodiments of the present invention minimize [minimizes] the growth of IC die size solely to provide adequate trace escape density on substrates. Embodiments of the [The] present invention also reduce [reduces] the need to provide substrates having additional layers to accommodate IC's having high densities of interconnect terminals, thus reducing design and manufacturing costs.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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The paragraph beginning on page 17, line 16 is amended as follows:

As shown herein, the present disclosure [invention] can be implemented in a number of different embodiments, including an electronic package substrate, an electronic package, an electronic system, a data processing system, methods for forming a package substrate, and methods for packaging an IC on a substrate. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements.

The paragraph beginning on page 17, line 23 is amended as follows:

For example, while an embodiment of an IC is shown in which signal traces are provided around the periphery and in which power supply traces are provided at the die core, embodiments of the invention are [is] equally applicable to embodiments where signal traces and power supply traces are provided anywhere on the die. Moreover, embodiments of the invention are [is] applicable to improving escape density for traces performing any type of function, and they are [it is] not limited to improving escape density for traces conducting input/output signals.

The paragraph beginning on page 18, line 1 is amended as follows:

Further, embodiments of the present invention are [is] not to be construed as limited to use in ball grid array (BGA) packages, and they [it] can be used with any other type of IC packaging technology where the herein-described features of the present invention provide an advantage, e.g. pin grid array (PGA), land grid array (LGA), chip scale package (CSP), or the like.

The paragraph beginning on page 18, line 10 is amended as follows:

Embodiments of [The] present invention are [is] not to be construed as limited to any particular type of substrate or to any particular method of coupling an IC or IC package to a substrate.

The paragraph beginning on page 18, line 13 is amended as follows:

The shape or cross-section of individual bumps and vias can assume any geometrical form, such as squares, rectangles, circles, pentagons, hexagons, and so forth, and they could also assume any type of irregular geometric shape. Embodiments of [The] present invention can be used with trace patterns wherein the trace width is less than, equal to, or greater than the trace spacing.

The paragraph beginning on page 18, line 18 is amended as follows:

The terms "upper" and "lower" are to be understood as relative terms, and it should be understood that the scope of the disclosure [invention] includes corresponding elements in structures that may be inverted relative to those shown in the figures and described herein.

The paragraph beginning on page 18, line 22 is amended as follows:

The above-described choice of materials, geometry, and assembly operations can all be varied by one of ordinary skill in the art to optimize the performance of the electronic package. The particular implementation of embodiments of the invention is very flexible in terms of the orientation, size, number, and composition of its constituent elements. Various embodiments of the invention can be implemented using any one or more of various geometrical arrangements of substrate terminals or lands to achieve the advantages of the present disclosure [invention].

The paragraph beginning on page 18, line 29 is amended as follows:

FIGS. 1 through 8 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 1 and 4-11 are intended to illustrate various implementations of the disclosure [invention] that can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning on page 19, line 4 is amended as follows:

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve